

# DATA SHEET

## **74AHC259; 74AHCT259** 8-bit addressable latch

Product specification  
File under Integrated Circuits, IC06

2000 Mar 14

## 8-bit addressable latch

**74AHC259;  
74AHCT259**

### FEATURES

- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V  
CDM EIA/JESD22-C101 exceeds 1000 V
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Inputs accept voltages higher than  $V_{CC}$
- For AHC only: operates with CMOS input levels
- For AHCT only: operates with TTL input levels
- Specified from  $-40$  to  $+85$  °C and from  $-40$  to  $+125$  °C.

### DESCRIPTION

The 74AHC/AHCT259 are high-speed Si-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74AHC/AHCT259 are high-speed 8-bit addressable latches designed for general purpose storage applications in digital systems. The '259' are multifunctional devices capable of storing single-line data in eight addressable latches, and also 3-to-8 decoder and demultiplexer, with active HIGH outputs (Q0 to Q7), functions are available.

The '259' also incorporates an active LOW common reset ( $\overline{MR}$ ) for resetting all latches as well as an active LOW enable input ( $\overline{LE}$ ).

The '259' has four modes of operation as shown in the mode select table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.

In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the (D) input with all other outputs in the LOW state. In the reset mode all outputs are LOW and unaffected by the address (A0 to A2) and data (D) input. When operating the '259' as an address latch, changing more than one bit of the address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode.

The mode select table summarizes the operations of the '259'.

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74AHC259;  
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SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC	AHCT	
$t_{PHL}/t_{PLH}$	propagation delay D to Qn	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	4.1	4.1	ns
	An to Qn		5.3	5.5	ns
	$\overline{LE}$ to Qn		4.3	4.3	ns
	$\overline{MR}$ to Qn		3.9	3.9	ns
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	3.0	3.0	pF
$C_O$	output capacitance		4.0	4.0	pF
$C_{PD}$	power dissipation capacitance	$C_L = 50\text{ pF}$ ; $f = 1\text{ MHz}$ ; notes 1 and 2	13	17	pF

**Notes**

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts.

- The condition is  $V_I = \text{GND}$  to  $V_{CC}$ .

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## FUNCTION TABLE

See note 1.

OPERATING MODE	INPUTS						OUTPUTS								
	$\overline{\text{MR}}$	$\overline{\text{LE}}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L	
demultiplexer (active HIGH 8-channel) decoder (when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L	
			d	H	L	L	L	Q = d	L	L	L	L	L	L	
			d	L	H	L	L	L	L	Q = d	L	L	L	L	L
			d	H	H	L	L	L	L	L	L	Q = d	L	L	L
			d	L	L	H	L	L	L	L	L	L	Q = d	L	L
			d	H	L	H	L	L	L	L	L	L	L	Q = d	L
			d	H	H	H	L	L	L	L	L	L	L	L	L
memory (do nothing)	H	H	X	X	X	X	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>	
addressable latch	H	L	d	L	L	L	Q = d	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>	
			d	H	L	L	q <sub>0</sub>	Q = d	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>	
			d	L	H	L	q <sub>0</sub>	q <sub>1</sub>	Q = d	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>	
			d	H	H	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	Q = d	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>	
			d	L	L	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	Q = d	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>	
			d	H	L	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	Q = d	q <sub>6</sub>	q <sub>7</sub>	
			d	L	H	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	Q = d	q <sub>7</sub>	
H	H	H	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	Q = d				

## Note

1. H = HIGH voltage level;

L = LOW voltage level;

X = don't care;

d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH  $\overline{\text{LE}}$  transition;

q = lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

## ORDERING INFORMATION

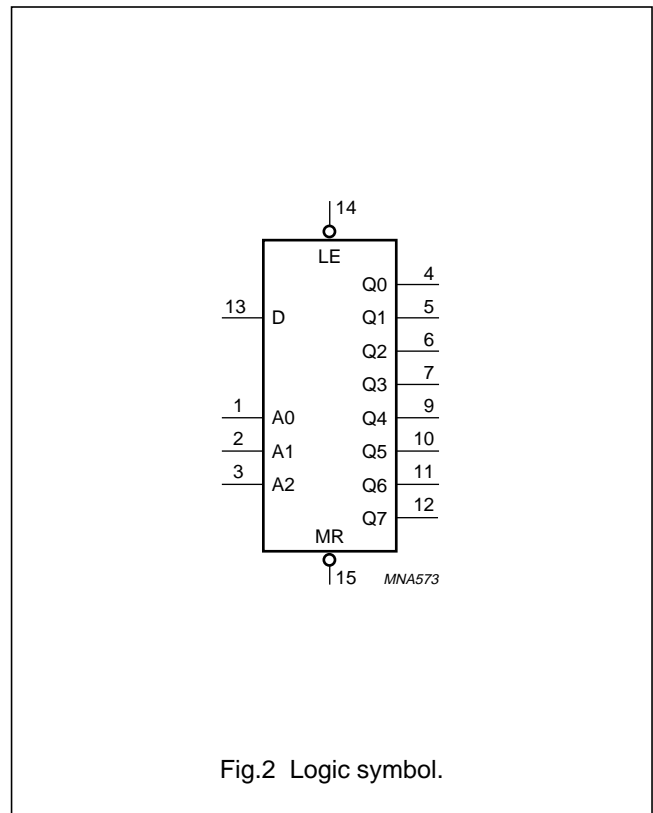
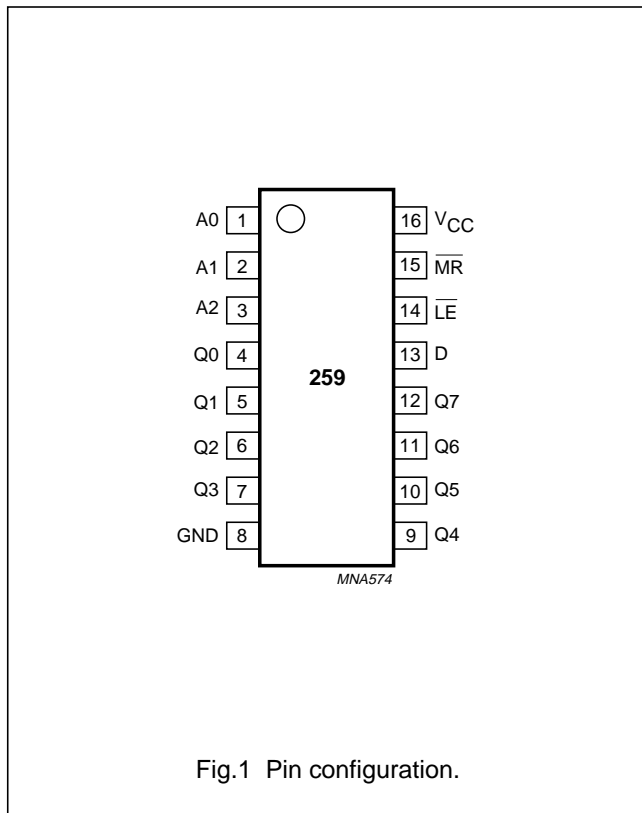
TYPE NUMBER	PACKAGES				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74AHC259D	-40 to +125 °C	16	SO	plastic	SOT109-1
74AHC259PW		16	TSSOP	plastic	SOT403-1
74AHCT259D		16	SO	plastic	SOT109-1
74AHCT259PW		16	TSSOP	plastic	SOT403-1

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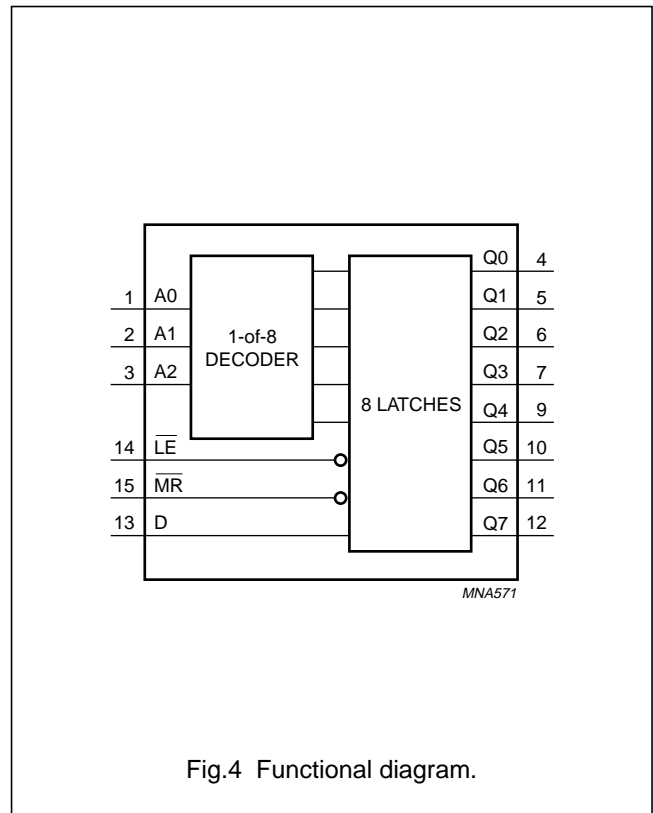
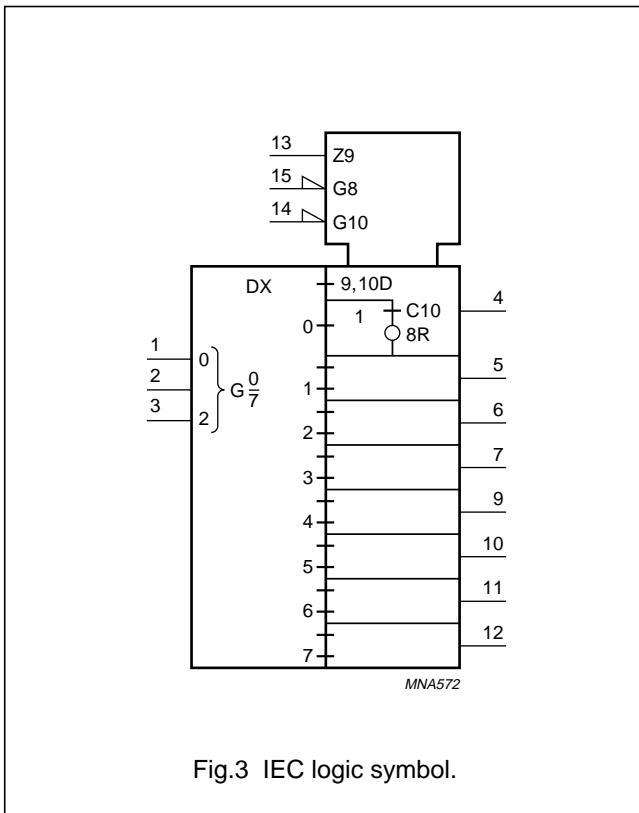
PINNING

PIN	SYMBOL	DESCRIPTION
1, 2 and 3	A0, A1 and A2	address input
4, 5, 6, 7, 9, 10, 11 and 12	Q0 to Q7	latch outputs
8	GND	ground (0 V)
13	D	data input
14	$\overline{LE}$	latch enable input (active LOW)
15	$\overline{MR}$	conditional reset input (active LOW)
16	V <sub>CC</sub>	DC supply voltage



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OPERATING MODE SELECT TABLE

LE	MR	MODE
L	H	addressable latch
H	H	memory
L	L	active HIGH 8-channel demultiplexer
H	L	reset

Note

- 1. H = HIGH voltage level;
- L = LOW voltage level.

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC			74AHCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$V_{CC}$	DC supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	–	5.5	0	–	5.5	V
$V_O$	output voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$T_{amb}$	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	+25	+125	–40	+25	+125	°C
$t_r, t_f$	input rise and fall ratios ( $\Delta t/\Delta f$ )	$V_{CC} = 3.3 \pm 0.3$ V	–	–	100	–	–	–	ns/V
		$V_{CC} = 5 \pm 0.5$ V	–	–	20	–	–	20	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	DC supply voltage		–0.5	+7.0	V
$V_I$	input voltage		–0.5	+7.0	V
$I_{IK}$	DC input diode current	$V_I < -0.5$ V; note 1	–	–20	mA
$I_{OK}$	DC output clamping diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1	–	$\pm 20$	mA
$I_O$	DC output sink current	$-0.5$ V $< V_O < V_{CC} + 0.5$ V	–	$\pm 25$	mA
$I_{CC}$	DC $V_{CC}$ or GND current		–	$\pm 75$	mA
$T_{stg}$	storage temperature		–65	+150	°C
$P_D$	power dissipation per package	for temperature range: –40 to +125 °C; note 2	–	500	mW

## Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO packages: above 70 °C the value of  $P_D$  derates linearly with 8 mW/K.  
For TSSOP packages: above 60 °C the value of  $P_D$  derates linearly with 5.5 mW/K.

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## DC CHARACTERISTICS

## 74AHC family

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)						UNIT	
		OTHER	V <sub>CC</sub> (V)	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	1.5	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	2.1	–	V
			5.5	3.85	–	–	3.85	–	3.85	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	–	0.9	V
			5.5	–	–	1.65	–	1.65	–	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -50 µA	2.0	1.9	2.0	–	1.9	–	1.9	–	V
			3.0	2.9	3.0	–	2.9	–	2.9	–	V
			4.5	4.4	4.5	–	4.4	–	4.4	–	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -4.0 mA	3.0	2.58	–	–	2.48	–	2.40	–	V
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -8.0 mA	4.5	3.94	–	–	3.8	–	3.70	–	V	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 50 µA	2.0	–	0	0.1	–	0.1	–	0.1	V
			3.0	–	0	0.1	–	0.1	–	0.1	V
			4.5	–	0	0.1	–	0.1	–	0.1	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4.0 mA	3.0	–	–	0.36	–	0.44	–	0.55	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 8.0 mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	0.1	–	1.0	–	2.0	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	–	–	±0.25	–	±2.5	–	±10.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	4.0	–	40	–	80	µA
C <sub>I</sub>	input capacitance		–	–	3	10	–	10	–	10	pF



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## 74AHCT family

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)						UNIT	
		OTHER	V <sub>CC</sub> (V)	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	2.0	–	2.0	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	–	0.8	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –50 µA	4.5	4.4	4.5	–	4.4	–	4.4	–	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –8.0 mA	4.5	3.94	–	–	3.8	–	3.70	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 50 µA	4.5	–	0	0.1	–	0.1	–	0.1	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 8.0 mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	5.5	–	–	0.1	–	1.0	–	2.0	µA
I <sub>oz</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND per input pin; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	±0.25	–	±2.5	–	±10.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	4.0	–	40	–	80	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0	4.5 to 5.5	–	–	1.35	–	1.5	–	1.5	mA
C <sub>I</sub>	input capacitance		–	–	3	10	–	10	–	10	pF

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AC CHARACTERISTICS

Type 74AHC259

GND = 0 V;  $t_r = t_f \leq 3.0$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)						UNIT	
		WAVEFORMS	C <sub>L</sub>	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
<b>V<sub>CC</sub> = 3.0 to 3.6 V; note 1</b>											
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay D to Qn	see Figs 5 and 11	15 pF	–	5.8	11.5	1.0	13.5	1.0	15.0	ns
	propagation delay An to Qn	see Figs 6 and 11		–	7.5	14.5	1.0	17.0	1.0	18.5	ns
	propagation delay $\overline{LE}$ to Qn	see Figs 7 and 11		–	6.2	12.0	1.0	14.0	1.0	15.2	ns
t <sub>PHL</sub>	propagation delay MR to Qn	see Figs 8 and 11		–	5.4	10.5	1.0	12.5	1.0	13.5	ns
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay D to Qn	see Figs 5 and 11	50 pF	–	7.3	14.5	1.0	17.0	1.0	18.5	ns
	propagation delay An to Qn	see Figs 6 and 11		–	9.1	18.0	1.0	21.0	1.0	23.0	ns
	propagation delay $\overline{LE}$ to Qn	see Figs 7 and 11		–	7.7	15.5	1.0	17.5	1.0	19.0	ns
t <sub>PHL</sub>	propagation delay MR to Qn	see Figs 8 and 11		–	7.0	13.5	1.0	15.5	1.0	17.0	ns
t <sub>w</sub>	$\overline{LE}$ pulse width HIGH or LOW	see Figs 7 and 11		5.0	–	–	5.0	–	5.0	–	ns
	$\overline{MR}$ pulse width LOW	see Figs 8 and 11		5.0	–	–	5.0	–	5.0	–	ns
t <sub>su</sub>	set-up time D to $\overline{LE}$ , An to $\overline{LE}$	see Figs 9, 10 and 11		4.0	–	–	4.0	–	4.0	–	ns
t <sub>h</sub>	hold time D to $\overline{LE}$ , An to $\overline{LE}$	see Figs 9 and 11		1.0	–	–	1.0	–	1.0	–	ns

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SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)						UNIT	
		WAVEFORMS	C <sub>L</sub>	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
<b>V<sub>CC</sub> = 4.5 to 5.5 V; note 2</b>											
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay D to Qn	see Figs 5 and 11	15 pF	–	4.1	7.5	1.0	9.0	1.0	10.0	ns
	propagation delay An to Qn	see Figs 6 and 11		–	5.3	9.5	1.0	11.5	1.0	12.5	ns
	propagation delay LE to Qn	see Figs 7 and 11		–	4.3	8.0	1.0	9.5	1.0	10.5	ns
t <sub>PHL</sub>	propagation delay MR to Qn	see Figs 8 and 11		–	3.9	7.0	1.0	8.5	1.0	9.5	ns
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay D to Qn	see Figs 5 and 11	50 pF	–	5.3	9.5	1.0	11.0	1.0	12.0	ns
	propagation delay An to Qn	see Figs 6 and 11		–	6.5	11.5	1.0	13.5	1.0	15.0	ns
	propagation delay LE to Qn	see Figs 7 and 11		–	5.5	10.0	1.0	11.5	1.0	12.5	ns
t <sub>PHL</sub>	propagation delay MR to Qn	see Figs 8 and 11		–	5.1	9.0	1.0	10.5	1.0	11.5	ns
t <sub>w</sub>	LE pulse width HIGH or LOW	see Figs 7 and 11		5.0	–	–	5.0	–	5.0	–	ns
	MR pulse width LOW	see Figs 8 and 11		5.0	–	–	5.0	–	5.0	–	ns
t <sub>su</sub>	set-up time D to LE, An to LE	see Figs 9, 10 and 11		4.0	–	–	4.0	–	4.0	–	ns
t <sub>h</sub>	hold time D to LE, An to LE	see Figs 9 and 11		1.0	–	–	1.0	–	1.0	–	ns

**Notes**

1. Typical values at V<sub>CC</sub> = 3.3 V.
2. Typical values at V<sub>CC</sub> = 5.0 V.

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## Type 74AHCT259

GND = 0 V;  $t_r = t_f \leq 3.0$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS		$T_{amb}$ (°C)						UNIT	
		WAVEFORMS	$C_L$	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
<b><math>V_{CC} = 4.5</math> to <math>5.5</math> V; note 1</b>											
$t_{PHL}/t_{PLH}$	propagation delay D to Qn	see Figs 5 and 11	15 pF	–	4.1	7.5	1.0	9.0	1.0	10.0	ns
	propagation delay An to Qn	see Figs 6 and 11		–	5.5	9.5	1.0	11.5	1.0	12.5	ns
	propagation delay $\overline{LE}$ to Qn	see Figs 7 and 11		–	4.3	8.0	1.0	9.5	1.0	10.4	ns
$t_{PHL}$	propagation delay MR to Qn	see Figs 8 and 11		–	3.9	7.0	1.0	8.5	1.0	9.5	ns
$t_{PHL}/t_{PLH}$	propagation delay D to Qn	see Figs 5 and 11	50 pF	–	5.4	9.5	1.0	11.0	1.0	12.0	ns
	propagation delay An to Qn	see Figs 6 and 11		–	6.6	12.0	1.0	14.0	1.0	15.5	ns
	propagation delay $\overline{LE}$ to Qn	see Figs 7 and 11		–	5.5	10.0	1.0	12.0	1.0	13.0	ns
$t_{PHL}$	propagation delay MR to Qn	see Figs 8 and 11		–	5.1	9.0	1.0	10.5	1.0	11.5	ns
$t_W$	$\overline{LE}$ pulse width HIGH or LOW	see Figs 7 and 11		5.0	–	–	5.0	–	5.0	–	ns
	$\overline{MR}$ pulse width LOW	see Figs 8 and 11		5.0	–	–	5.0	–	5.0	–	ns
$t_{su}$	set-up time D to $\overline{LE}$ , An to $\overline{LE}$	see Figs 9, 10 and 11		4.0	–	–	4.0	–	4.0	–	ns
$t_h$	hold time D to $\overline{LE}$ , An to $\overline{LE}$	see Figs 9 and 11	1.0	–	–	1.0	–	1.0	–	ns	

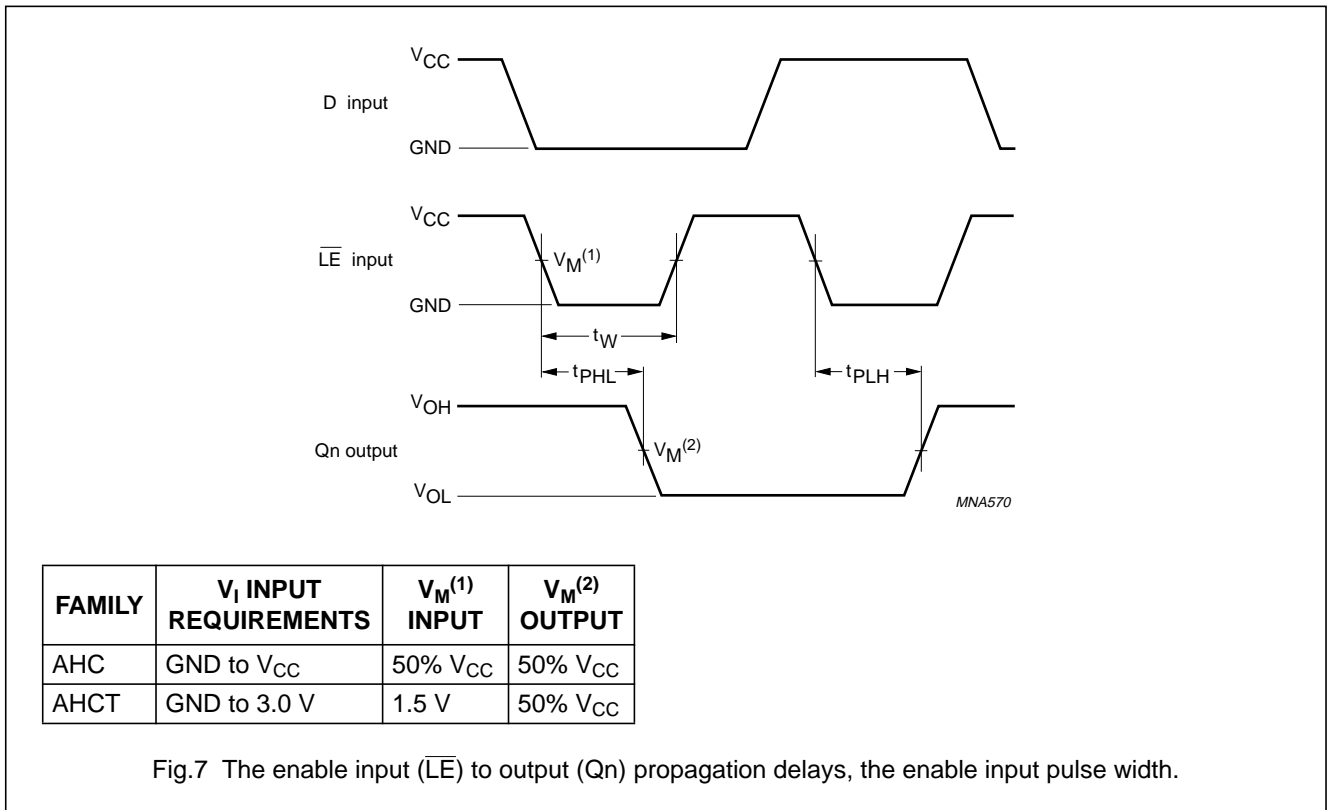
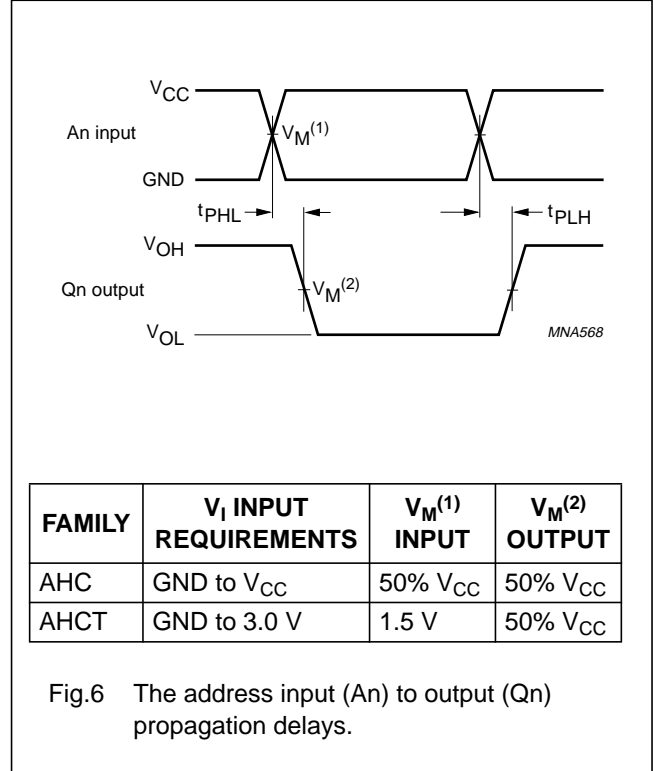
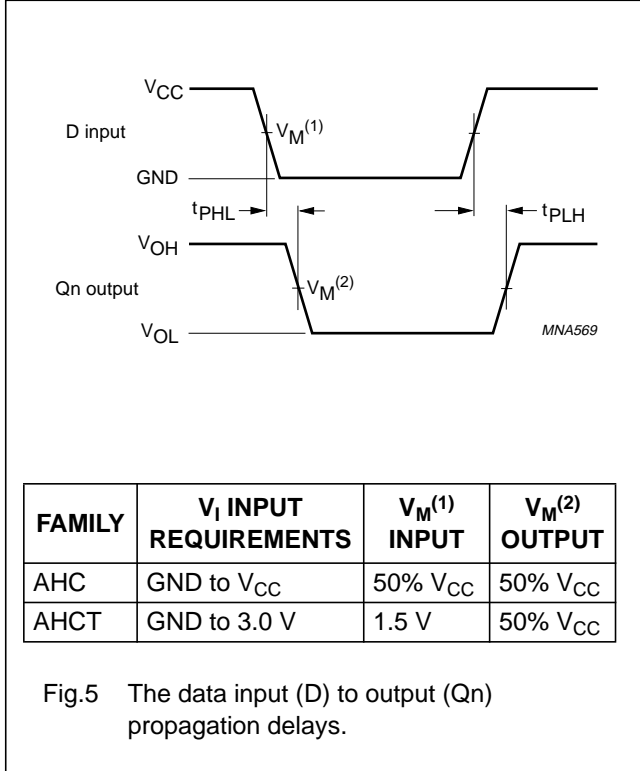
## Note

1. Typical values at  $V_{CC} = 5.0$  V.

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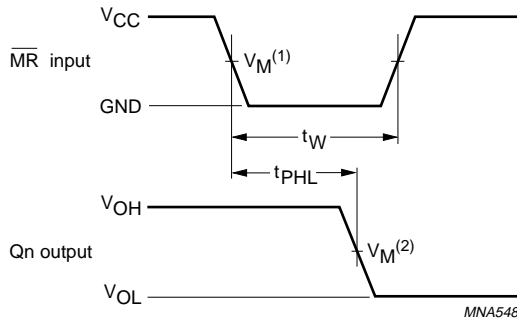
74AHC259;  
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AC WAVEFORMS



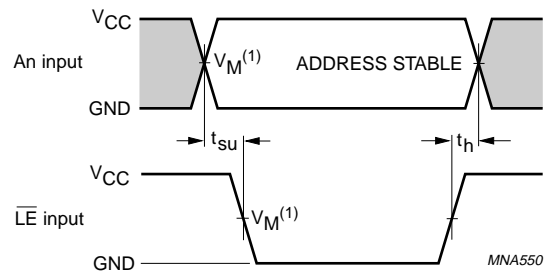
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FAMILY	V <sub>I</sub> INPUT REQUIREMENTS	V <sub>M</sub> <sup>(1)</sup> INPUT	V <sub>M</sub> <sup>(2)</sup> OUTPUT
AHC	GND to V <sub>CC</sub>	50% V <sub>CC</sub>	50% V <sub>CC</sub>
AHCT	GND to 3.0 V	1.5 V	50% V <sub>CC</sub>

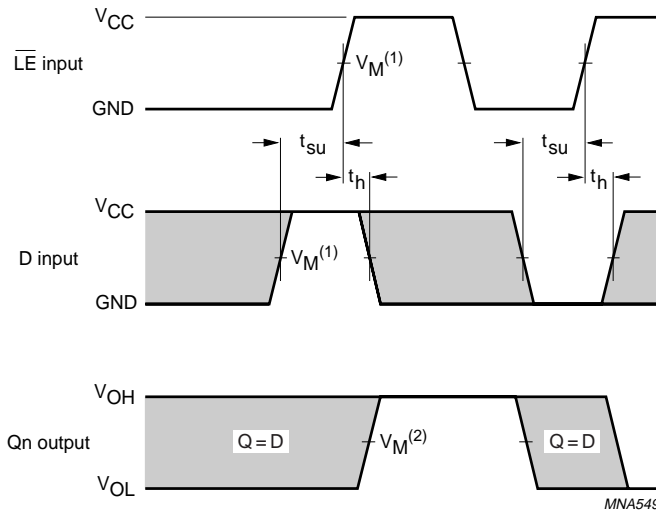
Fig.8 The conditional reset input ( $\overline{MR}$ ) to output ( $Q_n$ ) propagation delays.



The shaded areas indicate when the input is permitted to change for predictable output performance.

FAMILY	V <sub>I</sub> INPUT REQUIREMENTS	V <sub>M</sub> <sup>(1)</sup> INPUT
AHC	GND to V <sub>CC</sub>	50% V <sub>CC</sub>
AHCT	GND to 3.0 V	1.5 V

Fig.9 The address set-up and hold time for An inputs to  $\overline{LE}$  input.



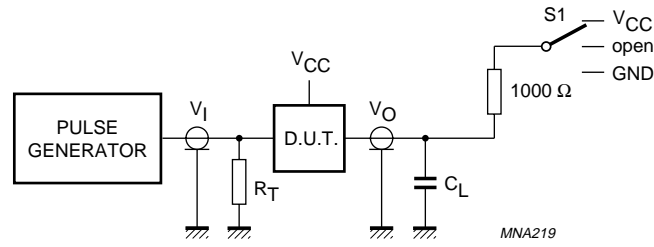
FAMILY	V <sub>I</sub> INPUT REQUIREMENTS	V <sub>M</sub> <sup>(1)</sup> INPUT	V <sub>M</sub> <sup>(2)</sup> OUTPUT
AHC	GND to V <sub>CC</sub>	50% V <sub>CC</sub>	50% V <sub>CC</sub>
AHCT	GND to 3.0 V	1.5 V	50% V <sub>CC</sub>

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.10 The data set-up and hold time for D input to  $\overline{LE}$  input.

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TEST	S1
$t_{PLH}/t_{PHL}$	open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

Definitions for test circuit.

$C_L$  = load capacitance including jig and probe capacitance (See Chapter "AC characteristics").

$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig.11 Load circuitry for switching times.

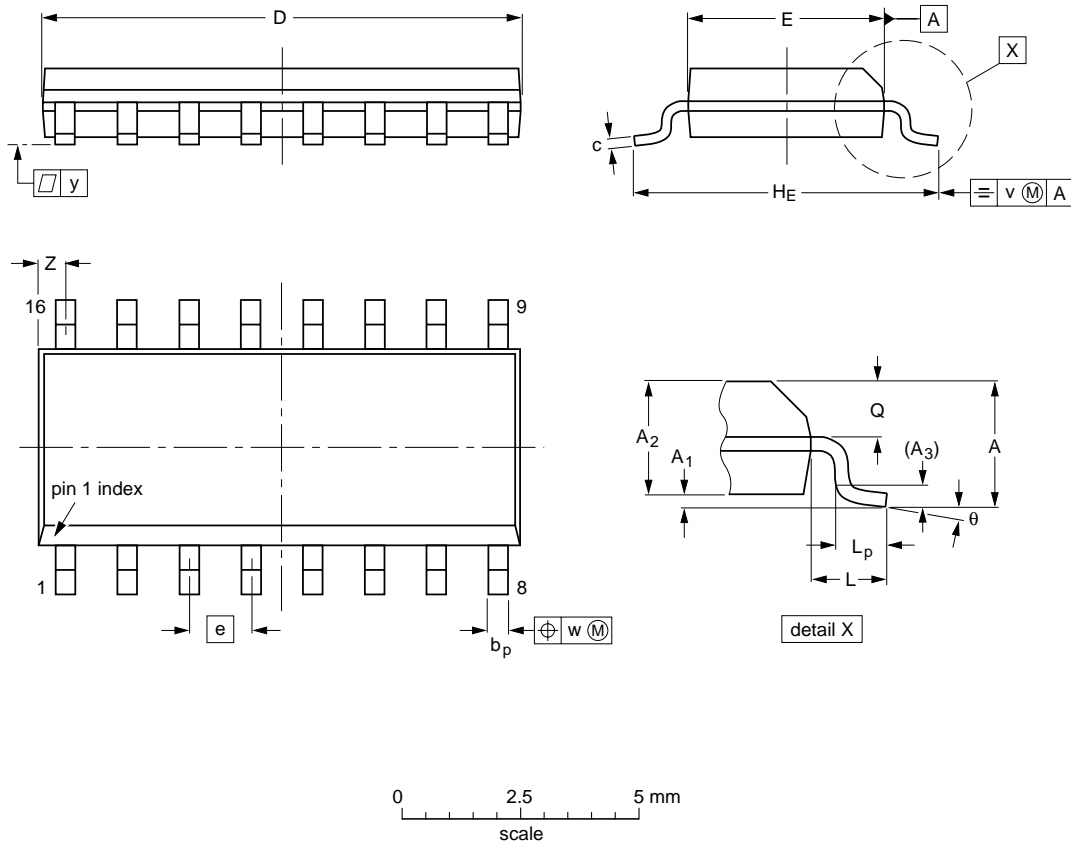
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PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				97-05-22 99-12-27

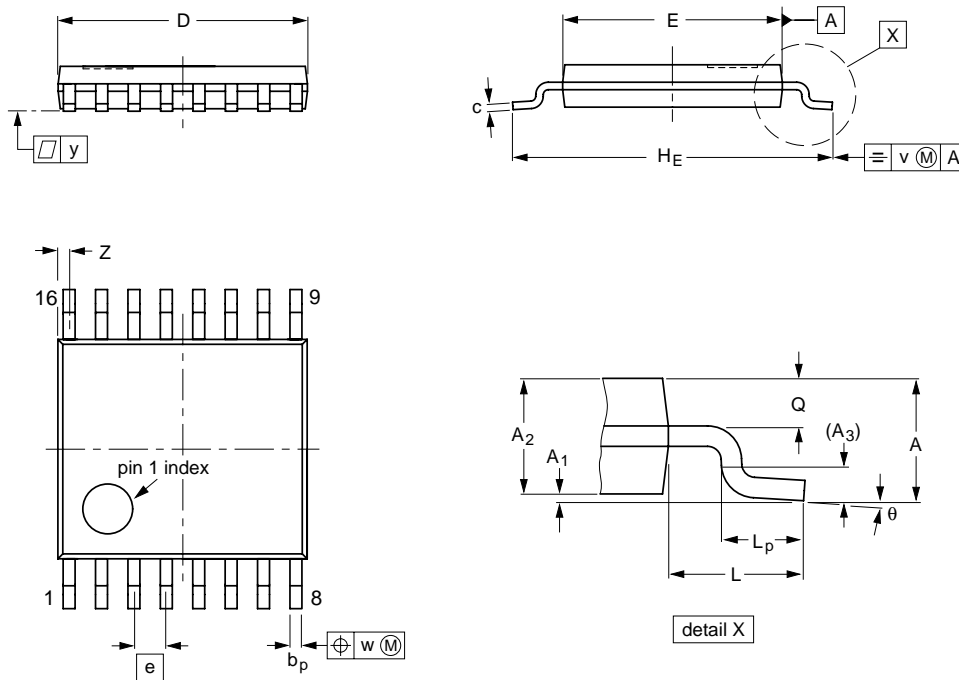


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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				-95-04-04 99-12-27

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### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 8-bit addressable latch

74AHC259;  
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## Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

## Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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